# Compact Modeling of Thin-Film Transistors for Flexible Hybrid IoT Design

**Leilai Shao**
University of California, Santa Barbara

**Ting Lei**
Stanford University

**Tsung-Ching Huang and Sicheng Li**
Hewlett Packard Labs

**Ta-Ya Chu**
National Research Council Canada

**Man Wong**
Hong Kong University of Science and Technology

**Raymond Beausoleil**
Hewlett Packard Labs

**Zhenan Bao**
Stanford University

**Kwang-Ting Cheng**
Hong Kong University of Science and Technology

*Editor's note:*
Thin-film transistors can be manufactured at low cost and on flexible materials using printing technologies. These characteristics make them very well suited to many IoT applications, particularly wearable electronics. However, circuit and system designers require device models for these new devices. This article describes a SPICE-compatible compact model for a range of thin-film transistors. The authors have validated the models on three thin-film transistor technologies.

*—Dimitrios Serpanos, University of Patras*
*—Marilyn Wolf, Georgia Institute of Technology*

**Flexible electronics is** emerging as an alternative to conventional silicon electronics for applications such as wearable sensors, artificial skin, medical patches, bendable displays, foldable solar cells, and disposable radio frequency identification tags [1], [2]. Unlike the conventional silicon electronics that needs sophisticated billion-dollar foundry for manufacturing, flexible electronic circuits can be fabricated on thin and conformable substrates, such as plastic films, with low-cost and high-throughput manufacturing methods, such as ink-jet printing and roll-to-roll imprinting. Therefore, the time to market as well as the manufacturing cost can be significantly reduced. Its flexible form factor also enables innovative designs for consumer electronics and biomedical applications [3], [4].

However, the circuit using pure flexible electronics suffers from slower operating speed and less reliability compared to CMOS technology. For sensing applications, such as touch, temperature, sweat, and bio-medical sensors [2], speed requirement is not critical, and thin-film transistor (TFT) technologies can operate at megahertz range to support such applications. Printing or solution compatible processes make the integration between the TFTs and the sensors much easier, and TFT itself also can be used for sensing [5]. Through heterogeneous integration of flexible devices and

*L. Shao, T. Leif, and T.-C. Huang contributed equally to this work.*

*Digital Object Identifier 10.1109/MDAT.2019.2899058*
*Date of publication: 12 February 2019; date of current version: 22 July 2019.*


2168-2356/19©2019 IEEE Copublished by the IEEE CEDA, IEEE CASS, IEEE SSCS, and TTTC

thinned silicon chips, we can bring low-cost sensing and high-performance computing to various connected "things" for wearables and Flex-Internet-of-Things (IoT) sensing nodes. A conceptual Flex-IoT sensing node is illustrated in Figure 1, where TFTs, sensors, and thinned silicon chips are integrated on the same flexible substrate.

There exist several challenges before Flex-IoT can be broadly employed for next-generation wearable and IoT products. Due to the material properties, TFTs are usually monotype, either only p- or only n-type devices [6]. Making air-stable complementary TFT circuits is quite challenging or often requires heterogeneous process integration of two different TFT technologies. Existing CMOS design methodologies for silicon electronics, therefore, cannot be directly applied for designing flexible electronics. Other factors, such as high supply voltages and large process variations, also make the designing of large-scale TFT circuits a significant challenge. To ease design challenges and perform technology evaluations, a trustworthy TFT compact model is needed to facilitate the simulations and design explorations.

Several TFT compact models targeting specific technologies [7] have been developed in the past that may not be generalized for other technologies. Some studies focus only on modeling the dc behavior [8], which does not support transient simulations. In this article, we present a unified compact model of TFTs covering dc, ac, and technology scaling factor for supporting Flex-IoT design and validate the model for three TFT technologies, i.e., carbon nanotube (CNT) TFTs, indium gallium zinc oxide (IGZO) TFTs, and organic thin film transistors (OTFTs). Based on this model, we further perform circuit-level validation based on fabricated Pseudo-CMOS inverters, sequence generators, and ring oscillators. The proposed model is implemented in Verilog-A, which is compatible with the SPICE simulation of CMOS circuitry and thus enables the designers to explore TFT-based flexible hybrid circuits and evaluate their potentials.

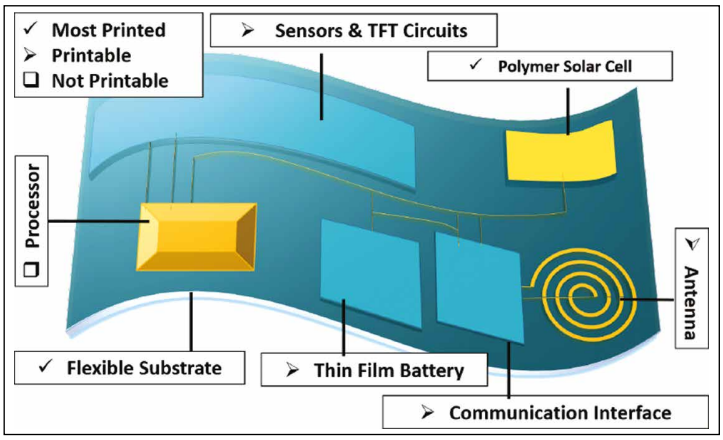


**Figure 1. Conceptual flexible hybrid IoT node.**

## Unified TFT model

### Observations and Motivations

To investigate the effective mobility of fabricated TFTs, low source–drain voltages ($V_{DS}$ = –0.5 $V$ and $V_{DS}$ = 0.1 $V$) are chosen for CNT–TFT and IGZO–TFT accordingly. The measured I–V curves are shown in the top part of Figure 2, and the bottom part shows the effective mobility $\mu_{eff}$. From Figure 2, we observed that the effective mobility $\mu_{eff}$ is enhanced as the $|V_{GS}|$ increases for both CNT–TFT and IGZO–TFT when $|V_{GS}|$ is relatively small. Similar mobility dependency phenomenon has been observed in OTFT and a-Si TFT [7], and the commonly accepted theories are based on the charge drift in the presence of tail-distributed traps (TDTs) and variable range hopping (VRH) [7]. This common phenomenon among different TFT technologies encourages us to build a unified model to capture fundamental behaviors of different TFTs based on TDTs and VRH assumptions.

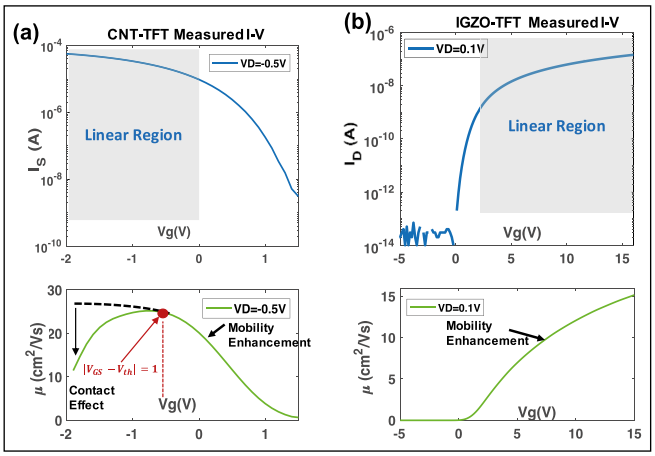


**Figure 2. Measured I–V curves and mobility dependency on gate voltages. (a) CNT–TFT with *L* = 25 *μm* and *W* = 125 *μm*. (b) IGZO–TFT *L* = 20 *μm* and *W* = 30 *μm*.**

## Assumptions and analysis

*1) Mobility enhancement:* Both theories indicate the field enhancement of mobility as

$$\mu = \begin{cases} \mu_0 (V_{\rm G} - V_{\rm th})^{\gamma}, & \text{N-type TFT} \\ \mu_0 (V_{\rm th} - V_{\rm G})^{\gamma}, & \text{P-type TFT} \end{cases}, \quad (1)$$

where $V_{\rm th}$ is the threshold voltage, $\gamma$ is the field enhancement factor for mobility, and $\mu_0$ is defined as the effective mobility when $|V_{\rm G} - V_{\rm th}| = 1$, as illustrated in Figure 2a. This mobility enhancement assumption explains the increase of the effective mobility at low $|V_{\rm GS}|$.

*2) Contact effect:* The degeneration of mobility at high $|V_{\rm GS}|$ can be explained partially by the contact resistances $R_S$ and $R_D$ at the source and drain terminals, respectively, as shown in Figure 3. These resistances result in effective gate-source/drain-source voltage drop: $\tilde{V}_{\rm GS} = V_{\rm GS} - R_S \tilde{I}_{\rm DS}$, $\tilde{V}_{\rm DS} = V_{\rm DS} - (R_S + R_D)\, \tilde{I}_{\rm DS} = V_{\rm DS} - R_C \tilde{I}_{\rm DS}$, where $R_C = R_S + R_D$ and the current with contact effect is denoted as $\tilde{I}_{\rm DS}$. The derivations are not presented here for simplicity, and the contact effect can be illustrated as

$$\tilde{I}_{\rm DS} \approx \frac{WC_{\rm ox}\mu}{L\{1 + kR_C(V_{\rm GS} - V_{\rm th})\}} \{(V_{\rm GS} - V_{\rm th}) - \frac{1}{2} V_{\rm DS}\} V_{\rm DS}, \quad (2)$$

$$\frac{\tilde{I}_{\rm DS}}{I_{\rm DS}} \approx \frac{\tilde{\mu}}{\mu} = \frac{1}{1 + kR_C(V_{\rm GS} - V_{\rm th})}; \quad k = \frac{W}{L} C_{\rm ox}\mu. \quad (3)$$

From (3), we can conclude that the contact resistances would lead to mobility reduction with a factor of $1/(1 + kR_c\,(V_{\rm GS} - V_{\rm th}))$, and it becomes more significant as $|V_{GS}|$ increases, which explains the degeneration of the effective mobility with a high $|V_{GS}|$ as shown in Figure 2a. For the devices shown in Figure 2, CNT–TFT has a relatively larger $k$ comparing to IGZO–TFT, $k_{\rm CNT} \approx 25 k_{\rm IGZO}$, thus leading to more obvious mobility degeneration.

*3) Surface roughness effect:* As gate voltage increases, the electrons tend to flow closer to the channel surface. Due to the low-cost fabrication process of TFTs, interface traps and surface roughness commonly exist, leading to the degeneration of the effective mobility [9].

$$\frac{\tilde{\mu}}{\mu} = \frac{1}{1 + \theta(V_{\rm GS} - V_{\rm th})} \quad (4)$$

Here, $\theta \propto 1/t_{\rm ox}$ is a parameter related to the thickness of the gate oxide layer. This phenomenon combining with the contact effect will lead to an overall mobility drop with a factor of $\approx 1/[1 + (\theta + kR_C)(V_{\rm GS} - V_{\rm th})]$. Although surface roughness and contact effect have an identical formula with a term proposal to $V_{GS} - V_{th}$, their physical explanations are different.

## Model derivations

We first establish the intrinsic current model based on the mobility enhancement assumption, and then we extend the model to capture parasitics and second-order effects.

*4) Intrinsic current model:* We integrate the mobility enhancement assumption (7) with the n-type charge drift model of (5) and (6) to derive the intrinsic current model [7].

$$I_{\rm DS(x)} = Q_{CH}(x)\, v;\, v = u_{\rm eff} \frac{\partial V(x)}{\partial x} \quad (5)$$

$$Q_{\rm CH}(x) = WC_{\rm ox}(V_G - V_{\rm th} - V(x)) \quad (6)$$

$$u_{\rm eff} = \mu_0 (V_G - V_{\rm th} - V(x))^{\gamma} \quad (7)$$

Since the current is constant in the channel [9], integrating along the channel $\int_{x=0}^{x=L} I_{\rm DS}(x)\,dx$ yields the following:

$$I_{\rm DS} = \frac{k}{(\gamma+2)} \{(V_{\rm GS} - V_{th})^{\gamma+2} - (V_{GD} - V_{th})^{\gamma+2}\}, \quad (8)$$

where $k$ is defined as $WC_{\rm ox}\mu_0/L$. Similar to MOSFET, we divide (8) into two regions: 1) linear and 2) saturation. Applying the Taylor expansion and keeping the first- and second-order terms, we can then simplify the formula as

$$I_{DS} \approx \begin{cases} k'\{V_{\rm GT} - \frac{1+\gamma}{2} V_{DS}\} V_{DS},\ V_{DS} \le V_{GT} \\ \frac{k'}{(\gamma+2)} V_{\rm GT}^2,\ V_{\rm DS} > V_{\rm GT} \end{cases} \quad (9)$$

$$k' = kV_{\rm GT}^{\gamma};\ V_{\rm GT} = V_{\rm GS} - V_{\rm th}. \quad (10)$$

Note that (9) becomes a conventional MOSFET model when $\gamma = 0$. This is because the main difference between the TFT intrinsic model, (8), and the MOSFET model is the mobility enhancement dependency on the gate voltage. This inherent connection between (8) and the MOSFET model leads to a major advantage, i.e., we can readily include second-order effects such as channel length modulation into (8), taking advantage of mature MOSFET theories.

*5) Extending the intrinsic model:* To further enrich the capability of the TFT intrinsic model,

we incorporate the channel length modulation $1 + \lambda V_{SD}$ and surface roughness effect into (8), and the limiting function $f_{\lim}(V_G,V)$ is added to provide smooth transitions between the subthreshold and the above-threshold regions [9].

$$I_{\mathrm{DS}} = \frac{k'\beta}{\gamma+2}\left(f(V_G,V_S)^{\gamma+2} - f(V_G,V_D)^{\gamma+2}\right)(1+\lambda V_{DS}), \quad (11)$$

$$f_{\lim}(V_G,V) = SS\ln\left[1+\exp\left(\frac{V_G - V_{th} - V}{SS}\right)\right]; \quad \beta = \frac{1}{1+\theta V_{GT}}, \quad (12)$$

where $\lambda$ is the channel length modulation factor and $SS$ is related to the subthreshold slope.

*6) Extrinsic contact resistance:* Two series resistances $R_S$ and $R_D$ are added to account for the contact effect, as shown in Figure 3. To accurately extract the contact resistance, we apply the transmission line method (TLM) to ~500 fabricated CNT–based devices, as shown in Figure 4. The total resistance $R_{total}$ of the two terminal test structure is composed of contact resistance $R_c = R_{cs} + R_{cd}$ and channel resistance $R_{ch}$. Here, $R_{ch}$ is the sheet resistance of the channel and $R_c = R_{cd} + R_{cs}$ is the unit width contact resistance.

$$R_{\mathrm{total}} = \frac{R_c}{W} + \frac{R_{\mathrm{ch}}L}{W} \quad (13)$$

Equation (13) indicates that the $R_{\mathrm{total}}$ is a linear function of $L$ if $W$ is kept as a constant. Figure 4 contains two critical parameters: 1) the unit width contact resistance ($R_c/W$ = 4.78 $k\Omega$) can be extracted from the intersection when $L = 0$ and 2) the minimum width ($W_{\min} \approx 2\ \mu m$) required for source/drain terminal can be extracted from the intersection when $R_{\mathrm{total}} = 0$. The extracted contact resistance will be used in our model and $W_{\min}$ for source/drain terminal will guide the device fabrications.

*7) Gate capacitance:* Two lumped capacitors $C_{GS}$ and $C_{\mathrm{GD}}$ are added to characterize the transient behavior of the TFT circuits. Due to the large device sizes (hundreds of micrometers scale), two lumped capacitors are sufficiently accurate to capture the transient responses of the TFT circuits. Gate source/drain parasitic capacitors $C_{GSO}$ and $C_{GDO}$ are also included to improve the accuracy.

$$C_{\mathrm{GS}} = C_{\mathrm{GCS}} + C_{\mathrm{GSO}};\quad C_{\mathrm{GD}} = C_{\mathrm{GCD}} + C_{\mathrm{GDO}} \quad (14)$$

$$C_{\mathrm{GSO}} = C_{\mathrm{GDO}} = C_{\mathrm{ox}}WL_{\mathrm{ov}} \quad (15)$$

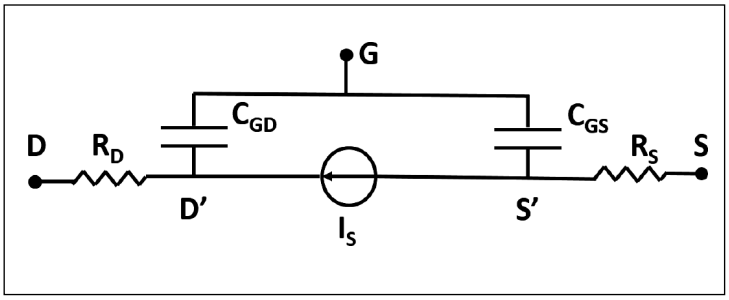


**Figure 3. TFT intrinsic model with contact resistances.**

$$C_{\mathrm{GCS}} = \frac{\partial Q_{\mathrm{CH}}}{\partial V_{\mathrm{GS}}} = \frac{2\,C_{\mathrm{ox}}\,WL}{3}\left[1-\left(\frac{V_{\mathrm{GT}}-V_{\mathrm{DSe}}}{2\,V_{\mathrm{GT}}-V_{\mathrm{DSe}}}\right)^2\right] \quad (16)$$

$$C_{\mathrm{GCD}} = \frac{\partial Q_{\mathrm{CH}}}{\partial V_{\mathrm{GD}}} = \frac{2\,C_{\mathrm{ox}}\,WL}{3}\left[1-\left(\frac{V_{\mathrm{GT}}}{2\,V_{\mathrm{GT}}-V_{\mathrm{DSe}}}\right)^2\right] \quad (17)$$

$$V_{\mathrm{DSe}} = \frac{1}{2}\left[V_{\mathrm{DS}} + V_{\mathrm{GT}} - \sqrt{V_\delta^2 + (V_{\mathrm{DS}} - V_{\mathrm{GT}})^2}\right], \quad (18)$$

where $L_{\mathrm{ov}}$ is the gate source/drain overlap and $V_\delta$ is a small number ($\sim 10mV$) to improve convergence. $C_{\mathrm{GCS}}$ and $C_{\mathrm{GCD}}$ are adapted from the Meyer capacitance model, and the typical gate voltage-dependent behaviors are shown in Figure 7a. The final equivalent circuit model is shown in Figure 3, and all equations can be implemented in Verilog-A for SPICE simulations.

## Model validations

In this section, we compare the SPICE simulation results with the measured drain–source current versus gate voltage (I–V) curves from CNT–TFT, IGZO–TFT, and OTFT. Additionally, the circuit-level validations are performed with fabricated Pseudo-CMOS inverters and ring oscillators [1].

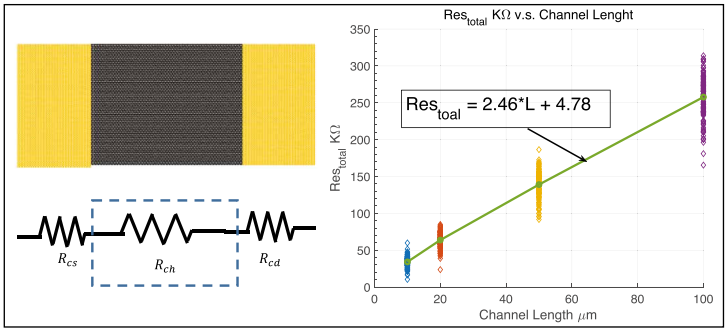


**Figure 4. Contact resistance TLM extrapolation based on ~500 fabricated devices with $L$ = 10, 20, 50, 100 $\mu m$ and $W$ = 40 $\mu m$.**

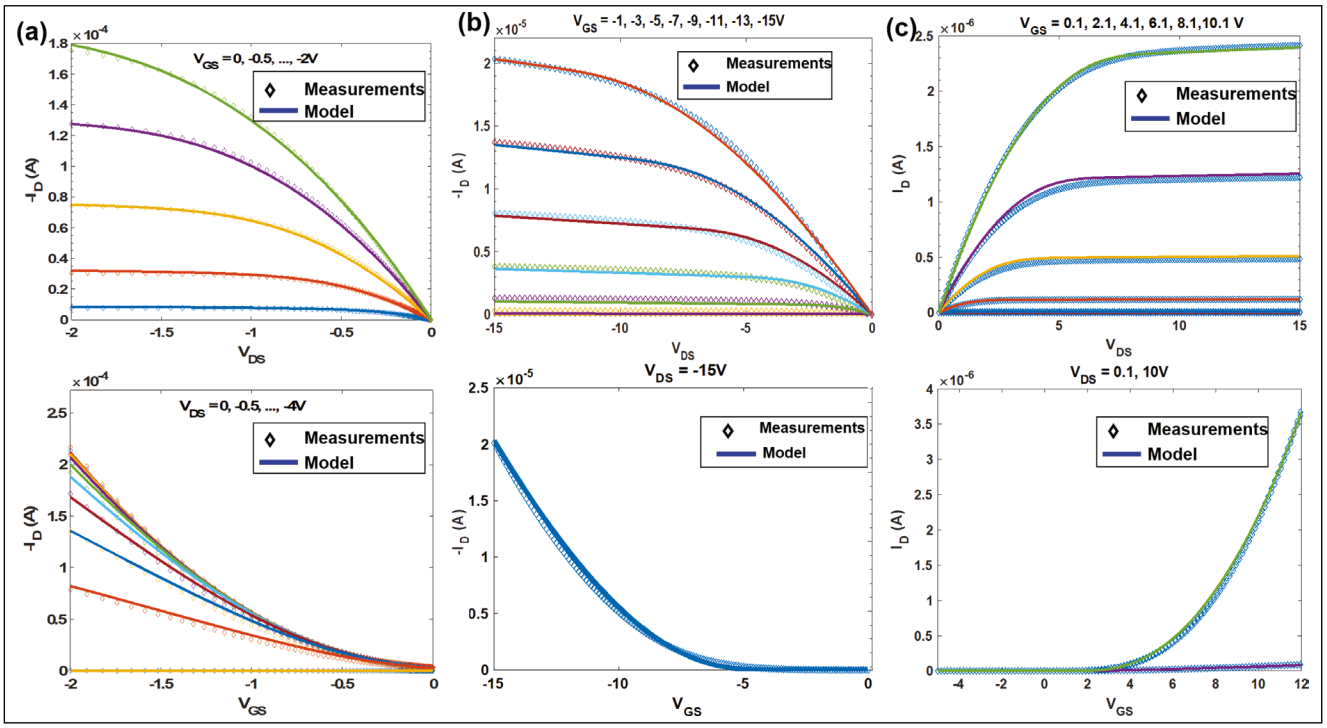


**Figure 5. Validations of the unified TFT model with measured *I–V* curves. (a) CNT–TFT with *W* = 125 *μm* and *L* = 25 *μm* [10]. (b) OTFT with *W* = 5000 *μm* and *L* = 10 *μm* [11]. (c) IGZO TFT with *W* = 30 *μm* and *L* = 20 *μm* [12].**

## Device validation

As shown in Figure 5, we first examined the unified TFT compact model with three measured I–V curves from CNT, IGZO, and organic TFTs. It can be seen that the model is able to accurately predict the dc behaviors of different TFTs, which well demonstrate the broad applicability of the unified compact model. The excellent match between the model predictions and the measurement data further confirm the validity of the above-mentioned model derivations and assumptions. We extracted the model parameters for three types of TFTs listed in Table 1. For CNT–TFTs, 52 devices' statistical information are also included and a Gaussian distribution is assumed for process variations, where the mean value $\mu$ and standard deviation $\sigma$ are shown.

**Table 1. Extracted parameters for CNT, IGZO, and organic TFTs.**

| Notation (Unit) | CNT-TFT [$\mu$, $\sigma$] | IGZO-TFT [$\mu$] | OTFT [$\mu$] |
|---|---|---|---|
| $L$ $(um)$ | [25, -] | 20 | 10 |
| $W$ $(um)$ | [125, -] | 30 | 5000 |
| $L_{ov}$ $(um)$ | [10, -] | 10 | 20 |
| $C_{ox}$ $(nF/cm^2)$ | [200, -] | 70 | 15 |
| $V_{th}$ $(V)$ | [0.5, 0.102] | 1.9 | -4.2 |
| $SS$ $(V/dec)$ | [0.28, 0.0388] | 0.8 | 0.6 |
| $\mu_0$ $(cm^2/Vs)$ | [25.69, 0.19] | 1.6 | 0.02 |
| $R_C$ $(\Omega)$ | [1531, 291] | 2500 | 80000 |
| $\lambda$ $(V^{-1})$ | [0.064, 0.0185] | 0.002 | 0.028 |
| $\gamma$ (-) | [0.20, 0.116] | 0.3 | 0.5 |
| $\theta$ $(V^{-1})$ | [0.01, 0.002] | 0.005 | 0.002 |

Field-effect mobility extracted based on an idealized MOSFET current model has been widely used for TFT performance benchmarking. With the field-dependent properties, the extracted mobility could vary significantly at different effective gate voltage bias. Therefore, to fairly evaluate the performance of a TFT, a combination of the low field-effect mobility ($\mu_0$) and field-dependent factor ($\gamma$) should be used to fairly evaluate the mobility performance. Thus, the unified compact model enables accurate simulation and also serves as a benchmark for technology evaluations.

## Circuits validation

Beside single devices, the model must be able to predict the circuit-level behaviors with high accuracy. We, therefore, compare the SPICE simulation results with the measured voltage transfer curves (VTCs), rising/falling times, and ring oscillators' waveform.

*1) Introduction to Pseudo-CMOS:* Pseudo-CMOS is a design style proposed to address the challenges of TFT circuit design based on monotype devices [1], which has been proven a robust design style for flexible digital, analog, and power circuits. Compared to conventional monotype digital design styles, such as the diode-load or resistive-load designs, Pseudo-CMOS offers better noise margin and provides postfabrication tunability at the cost of an additional power rail $V_{SS}$. There are two topologies of Pseudo-CMOS: Depletion (Pseudo-D) type and enhancement (Pseudo-E) type. Both Pseudo-D and Pseudo-E inverters' schematics are shown in Figure 6a and b, respectively, which consist of three power rails, $V_{DD}$, $V_{SS}$, and GND, and four transistors $M_{1–4}$.

*2) VTC validation:* In Figure 6c, we compare the SPICE-simulated VTCs with actual measurement data, where the solid lines represent the SPICE simulations and dots represent the measurements. Simulated VTCs match closely with the circuit measurements over a wide range of supply voltages $V_{DD}$, from 0.8 to 1.6 V. Despite minor discrepancies in low supply voltages, the proposed model accurately predicts the DC behaviors of a Pseudo-D inverter. In Figure 6d, 26 Pseudo-D inverters' VTCs are plotted together and the SPICE simulations (bold lines) can accurately predict the average behaviors of the VTCs using the mean values in Table 1.

*3) Dynamic validation:* We validated our ac model using the Pseudo-CMOS inverter's rising/falling times, ring oscillators' measured waveforms, and sequence generator's dynamic behaviors. To analyze the circuit variations, we first conducted a case study on the Pseudo-E inverter's dynamic behaviors after taking the variations into considerations. Monte Carlo simulations were performed with standard variation, summarized in Table 1 of CNT–TFTs. As shown in Figure 6e–h, our model can indeed capture the dynamic behaviors and variations of Pseudo-E inverters, as evident by good match to the results of fabricated CNT-TFT-based devices.

For transient validations, as shown in Figure 7a and b, with the developed dc and capacitance models, the transient simulation result well captures the oscillation frequency and the amplitude, compared with the measurement data. Also, we designed and tested 34 five-stage ring oscillators in a 4-inch wafer with their statistics summarized in Figure 7c. Overall, 500 Monte Carlo simulations are performed with the developed model, and the statistical simulation results show less than 10% errors compared to the physical measurements as indicated in Figure 7c and d. These errors are mainly caused by

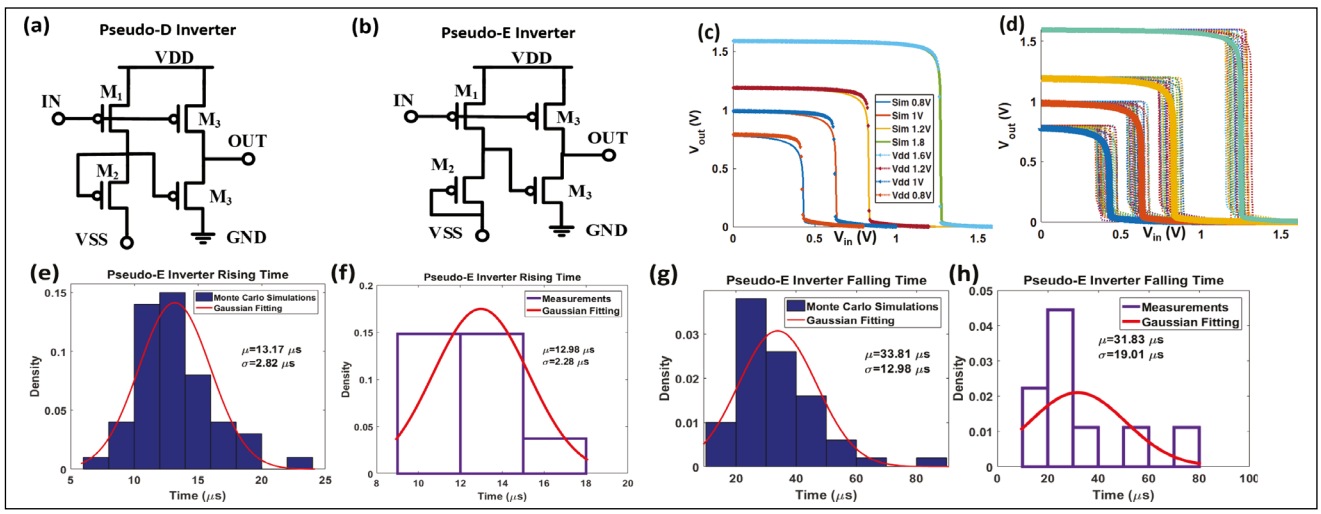


**Figure 6. (a) and (b) Schematic of a Pseudo-D/-E inverter. (c) Dot lines: Measured VTCs for a CNT–TFT-based Pseudo-D inverter with $V_{DD}$ = 1.6, 1.2, 1.0, and 0.8 V; solid lines: model predictions. (d) Dot lines: 26 measured VTCs of CNT-TFT-based Pseudo-D inverter with $V_{DD}$ = 1.6, 1.2, 1.0, and 0.8 V; solid lines: model predictions with extracted parameters in Table 1. (e) Fifty Monte Carlo simulations of Pseudo-E inverters' rising time. (f) Ten measured Pseudo-E inverters' rising time. (g) Fifty Monte Carlo simulations of Pseudo-E inverters' falling time. (h) Ten measured Pseudo-E inverters' falling time. L = 25 *μm* for above measurements.**

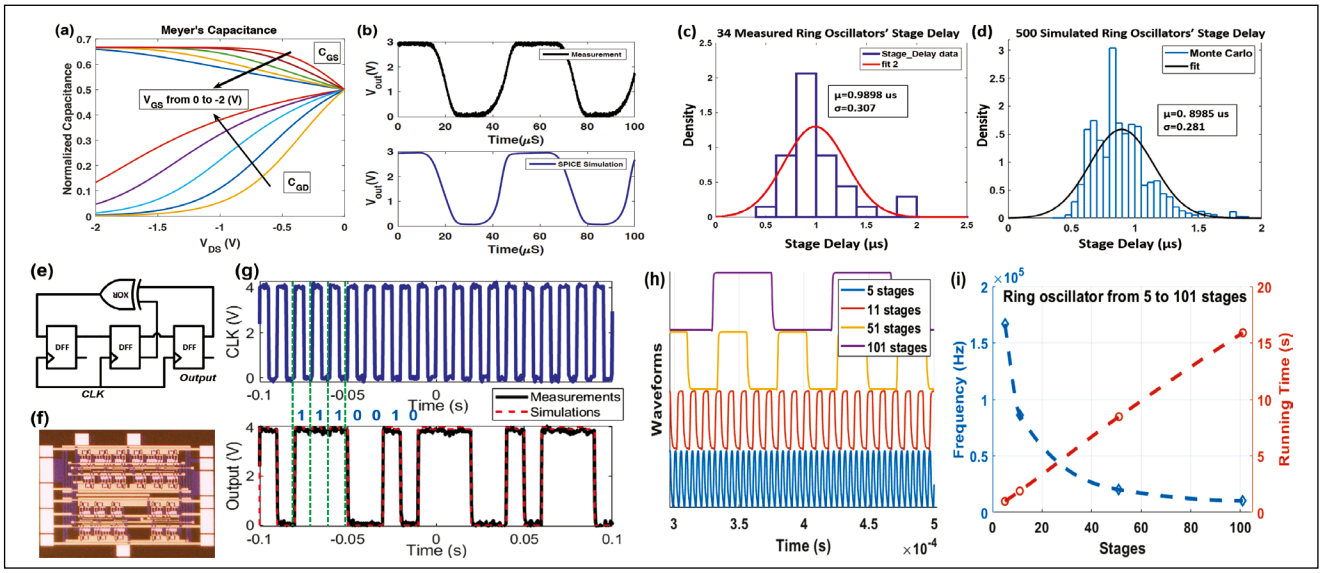


**Figure 7. (a) Meyer capacitance model for p-type devices. (b) SPICE simulated five-stage ring oscillators' waveform versus measured waveform; L = 25 *μm*. (c) Thirty-four measured five-stage Pseudo-D ring oscillators' stage delay. L = 2 *μm*. (d) Five hundred Monte Carlo simulations of ring oscillators' stage delay. (e) and (f) Schematic and die photograph of a 3-bit maximum-length linear LFSR composed of three D-flip flops and one XOR gate. (g) Measurements and simulation results of a fabricated sequence generator ("1110010") with CLK = 100 Hz, *L* = 10 *μm*, $V_{DD}$ = 4 V, and $V_{SS}$ = −4 V. (h) Waveforms of ring oscillators from 5 to 101 stages. (i) Simulated frequency and running time versus stages with a total of 500-*μs* simulation time and a 200-ns time step.**

the device and interconnect parasitics, which will be discussed in the next section and could be an important future work. Furthermore, we designed, fabricated, and tested a linear-feedback shift register (LFSR)-based sequence generator, which can be applied in signature generation, cryptography, and test-pattern generation, as shown in Figure 7e and f. The sequence generator contains 200 CNT–TFTs, and our model is able to accurately predict the outcome of such a medium-scale circuit, as indicated in Figure 7g, which further demonstrates our model's capability to predict relative complex circuitry's behaviors.

For large-scale circuit designs, model's stability and scalability are crucial. We examined these aspects of our model with HSpice and Spectre simulators using ring oscillators as a test bench. Simulation results from the two simulators are consistent with each other. Transient waveform, frequency, and running time of ring oscillators from 5 to 101 stages are summarized in Figure 7h and i. All ring oscillators show fast convergence, and the running time shows a linear relationship with the circuit complexity, which indicates the good stability and scalability of the developed compact model.

At the device level, validations have been conducted for three different TFT technologies. At the circuit level,we compared the model predictions with fabricated Pseudo-CMOS circuits. In summary, the good match between the model and measurements of both dc and the transient simulations indicate that the developed unified TFT model can accurately predict both device and circuit-level behaviors.

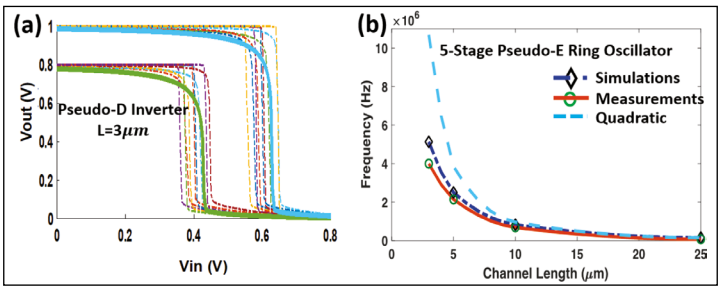


**Figure 8. (a) Dot lines: six CNT-TFT-based Pseudo-D inverter's VTCs with channel length L = 3 *μm*; solid line: model predictions for Pseudo-D inverter. (b) Model prediction of CNT–TFT-based five-stage ring oscillators' frequency versus measured frequency.**

## Technology scaling

In this section, we further investigate the channel length scaling effect. First, we compared the model predictions of a Pseudo-D inverter with measurements of six fabricated circuits with a channel length of 3 $\mu m$. As shown in Figure 8a, the comparison between the dc simulation and the circuit measurements for Pseudo-D inverters shows a good correlation for channel length down to 3 $\mu m$. For ac behaviors, a five-stage Pseudo-E-based ring oscillator is used as a vehicle for investigating the scaling effect. Both the model predictions and the measurements of ring oscillator's frequency are shown in Figure 8b. Both simulations and measurements show that the frequency does not increase quadratically as the channel length decreases. This is due to the nonnegligible device parasitics, such as contact resistance and parasitic gate capacitance. Another observation is that as the channel length decreases, the deviation of model predictions from the measurements grows. This phenomenon is due to the nontrivial interconnect parasitics. For instance, a printed wire's sheet resistance could be as large as ~1 ohm/square. Also, a typical TFT process only has two to three metal layers, which inevitably will increase the overlap between the layers causing significant parasitic capacitance. Thus, for high-performance TFT circuit design, accurate interconnect model and layout parasitic extraction are necessary to better capture the circuit behaviors. This would be an important subject for future study to further improve the accuracy of the simulation results.

**In this article,** we presented a unified TFT model for flexible hybrid IoT circuit and system design. The proposed model has been validated using three different TFT technologies and several Pseudo-CMOS circuits, covering both dc and ac behaviors. Also, we investigated the technology scaling effect with channel scaled from 25 to 3 $\mu m$. The analysis and measurement indicated that the device parasitics should be carefully optimized to approach the ideal quadratic improvement with channel length scaling. We further identified that the interconnect parasitics should be included to further improve the simulation accuracy. ■

## Acknowledgment

The work described in this article was partially supported by a grant from Research Grants Council of Hong Kong.

## ■ References

[1] T.-C. Huang, K. Fukuda, T. Someya, and K.-T. Cheng, "Pseudo-CMOS: A design style for low-cost and robust flexible electronics," *IEEE Trans. Elect. Dev.,* vol. 58, no. 1, pp. 141–150, 2011.

[2] S. Wang et al., "Skin electronics from scalable fabrication of an intrinsically stretchable transistor array," *Nature*, vol. 555, no. 7694, p. 83, 2018.

[3] C. Wang et al., "User-interactive electronic skin for instantaneous pressure visualization," *Nat. Mater.,* vol. 12, no. 10, pp. 899–904, 2013.

[4] T. Lei et al., "Biocompatible and totally disintegrable semiconducting polymer for ultrathin and ultralightweight transient electronics," *Proc. Nat. Acad. Sci.,* vol. 114, no. 20, pp. 5107–5112, 2017.

[5] C. Zhu et al., "Stretchable temperature-sensing circuits with strain suppression based on carbon nanotube transistors," *Nat. Electron.,* vol. 1, no. 3, p. 183, 2018.

[6] T.-C. Huang, L. Shao, T. Lei, R. Beausoleil, Z. Bao, and K.-T. Cheng, "Robust design and design automation for flexible hybrid electronics," in *Proc. 2017* IEEE Int. *Symp. Circ. Syst.*, pp. 1–4.

[7] O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, "Organic thin-film transistors: Part i—compact dc modeling," *IEEE Trans. Elect. Dev.,* vol. 56, no. 12, pp. 2952–2961, 2009.

[8] J. Zhao et al., "Universal compact model for thin-film transistors and circuit simulation for low-cost flexible large area electronics," *IEEE Trans. Elect. Dev.,* 2017.

[9] Y. Tsividis and C. Me Andrew, *Operation and Modeling of the MOS Transistor.* Oxford University Press, 2011.

[10] L. Shao, T.-C. Huang, T. Lei, Z. Bao, R. Beausoleil, and K.-T. Cheng, "Compact modeling of carbon nanotube thin film transistors for flexible circuit design," in *Proc. 2018 IEEE* Des. *Autom. Test Europe Conf. Exhibition*, pp. 491–496.

[11] T.-Y. Chu, Z. Zhang, A. Dadvand, C. Py, S. Lang, and Y. Tao, "Direct writing of inkjet-printed short channel organic thin film transistors," *Org. Electron.,* vol. 51, pp. 485–189, 2017.

[12] L. Lu, J. Li, H. S. Kwok, and M. Wong, "High-performance and reliable elevated-metal metal-oxide thin-film transistor for high-resolution displays," in *Proc. 2016* IEEE Int. *Elect. Dev. Meeting*, p. 32–2.

**Leilai Shao** is currently pursuing a PhD in electrical and computer engineering from the SOC Design and Test Lab, University of California, Santa Barbara, CA. His research interests include flexible hybrid electronics (FHE), machine learning

and abnormal detection for IoT, and wearable and biomedical applications. Shao has a BE in electronics and information engineering from Zhejiang University, Chu Kochen College, China.

**Ting Lei** is an Assistant Professor with the Department of Materials Science and Engineering, Peking University, China. His research interests include organic and polymer functional materials, organic electronics, carbon-based electronics, and bioelectronics. Lei has a BS and a PhD from Peking University (2008 and 2013, respectively).

**Tsung-Ching Huang** is a Senior Research Scientist with Hewlett Packard Labs, Palo Alto, CA. He is a Senior Member of the IEEE and a NextFlex Fellow.

**Sicheng Li** is a Research Associate with Hewlett Packard Labs, Palo Alto, CA. His research interests include reconfigurable computing, efficient and scalable machine learning, and neuromorphic computing. Li has an MS from New York University and a PhD from the University of Pittsburgh (2013 and 2017, respectively), both in electronic engineering.

**Ta-Ya Chu** is the Project Leader for the development of printed OTFTs and logic circuits with the National Research Council Canada, Ottawa, ON, Canada. Chu has an MSc in physics from Tamkang University, Taipei, Taiwan (1999) and a PhD in electrophysics from National Chiao Tung University, Hsinchu, Taiwan (2006). He is a Senior Member of the IEEE.

**Man Wong** is a Faculty Member with the Hong Kong University of Science and Technology, Hong Kong. Wong has a PhD in electrical engineering from Stanford University, Palo Alto, CA. He is a Senior Member of the IEEE.

**Raymond G. Beausoleil** is currently a Senior Fellow and Senior Vice President at Hewlett Packard Enterprise (HPE), San Jose, CA, and an Adjunct Professor of Applied Physics with Stanford University, Stanford, CA. Beausoleil has a BS from Caltech, Pasadena, CA (1980), and a PhD from Stanford University, Stanford, CA (1986), both in physics. He is a fellow of the American Physical Society and the Optical Society of America.

**Zhenan Bao** is a K.K. Lee Professor of chemical engineering with Stanford University, Stanford, CA. Bao has a PhD in chemistry from the University of Chicago (1995). She is a member of the National Academy of Engineering and the National Academy of Inventors.

**Kwang-Ting Cheng** is Dean of Engineering at the Hong Kong University of Science and Technology. His research interests include testing, design, and automation for VLSI, photonics IC, flexible hybrid circuits, and memristive memories, especially on computer vision and medical image analysis. Cheng has a PhD from the University of California, Berkeley, CA. He is a Fellow of the IEEE.

■ Direct questions and comments about this article to Leilai Shao, Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA; lshao@ece.ucsb.edu.